SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2015-178458; filed on September 10, 2015; the entire contents of which are incorporated herein by reference.

FIELD

Embodiments described herein relate generally to a semiconductor device.

BACKGROUND

There is a vertical metal oxide semiconductor field effect transistor (MOSFET) in which a p type (or n type) semiconductor layer is buried in an n type (or p type) semiconductor layer, and which has a super junction structure (hereinafter, also referred to as a SJ structure) having an n type region and a p type region that are alternately arranged, as a semiconductor device for power control with a high breakdown voltage and a low ON resistance. In the SJ structure, the amount of n type impurities which is included in the n type region is equal to the amount of p type impurities which is included in the p type region, and thereby a non-doped region is simulatively formed and a high breakdown voltage is achieved. Since impurity concentration of a semiconductor layer is increased by an increase of the breakdown voltage of the semiconductor device, it is possible to realize an increase of the breakdown voltage and a low ON resistance.

A method for forming the SJ structure includes, for example, a method in which a trench is formed in an n type semiconductor layer, a p type semiconductor is buried in the trench, and thereby a p type semiconductor layer is formed. However, in this method, a hollow portion (empty hole, void) is easily formed inside a p type semiconductor layer.

An example of related art includes JP-A-2014-075402.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic sectional view of a semiconductor device according to a first embodiment.

FIG. 2 is a schematic sectional view of the semiconductor device in the process of fabrication, based on a fabrication method of the semiconductor device according to the first embodiment.

FIG. 3 is a schematic sectional view of the semiconductor device in the process of the fabrication, based on the fabrication method of the semiconductor device according to the first embodiment.

FIG. 4 is a schematic sectional view of the semiconductor device in the process of the fabrication, based on the fabrication method of the semiconductor device according to the first embodiment.

FIG. 5 is a schematic sectional view of the semiconductor device in the process of the fabrication, based on the fabrication method of the semiconductor device according to the first embodiment.

FIG. 6 is a schematic sectional view of the semiconductor device in the process of the fabrication, based on the fabrication method of the semiconductor device according to the first embodiment.

FIG. 7 is a schematic sectional view of the semiconductor device in the process of the fabrication, based on the fabrication method of the semiconductor device according to the first embodiment.

FIG. 8 is a schematic sectional view of the semiconductor device in the process of the fabrication, based on the fabrication method of the semiconductor device according to the first embodiment.

FIG. 9 is a schematic sectional view of the semiconductor device in the process of the fabrication, based on the fabrication method of the semiconductor device according to the first embodiment.

FIG. 10 is a schematic sectional view of the semiconductor device in the process of the fabrication, based on the fabrication method of the semiconductor device according to the first embodiment.

FIG. 11 is a schematic sectional view of the semiconductor device in the process of the fabrication, based on the fabrication method of the semiconductor device according to the first embodiment.

FIG. 12 is a schematic sectional view of the semiconductor device in the process of the fabrication, based on the fabrication method of the semiconductor device according to the first embodiment.

FIG. 13 is a schematic sectional view of the semiconductor device in the process of the fabrication, based on the fabrication method of the semiconductor device according to the first embodiment.

FIG. 14 is a schematic sectional view of the semiconductor device in the process of the fabrication, based on the fabrication method of the semiconductor device according to the first embodiment.

FIG. 15 is a schematic sectional view of the semiconductor device in the process of the fabrication, based on the fabrication method of the semiconductor device according to the first embodiment.

FIG. 16 is a schematic sectional view of the semiconductor device in the process of the fabrication, based on the fabrication method of the semiconductor device according to the first embodiment.

FIG. 17 is a schematic sectional view of the semiconductor device in the process of the fabrication, based on the fabrication method of the semiconductor device according to the first embodiment.

FIG. 18 is a schematic sectional view of a semiconductor device according to a second embodiment.

DETAILED DESCRIPTION

[0005]Exemplary embodiments provide a semiconductor device which can suppress degradation of characteristics of a super junction structure.

[0006]In general, according to one embodiment, the semiconductor device includes a first conductive type semiconductor layer; a plurality of first regions which are positioned to alternate with a portion of the semiconductor layer in a first direction of the semiconductor layer, and includes a second conductive type impurity region; a second region which is positioned between the first regions in the first direction, and includes a first conductive type impurity region and a first insulator material that is positioned between the first conductive type impurity region and the semiconductor layer; and a third region which is provided between the first region and the second region, and includes a second insulator material.

[0008]Embodiments of the invention will be hereinafter descried with reference to the drawings. In the following description, the same symbols or reference numerals will be attached to the same members or the like, and description of the members or the like described once will be appropriately omitted.

[0009]In the specification, an upward direction of the drawing is referred to as “upper”, and a downward direction of the drawing is referred to as “lower”, in order to represent a positional relationship of components or the like. In the specification, concept of “upper” and “lower” is not necessarily the terms representing a relationship between directions of gravity.

First Embodiment

[0010]A semiconductor device according to the present embodiment includes a first conductive type semiconductor layer; a plurality of first regions which are positioned to alternate with a portion of the semiconductor layer in a first direction of the semiconductor layer, and includes a second conductive type impurity region; a second region which is positioned between the first regions in the first direction, and includes a first conductive type impurity region and a first insulator material that is positioned between the first conductive type impurity region and the semiconductor layer; and a third region which is provided between the first region and the second region, and includes a second insulator material.

[0011]FIG. 1 is a schematic sectional view of the semiconductor device according to the first embodiment. The semiconductor device 100 according to the present embodiment is a vertical MOSFET of a trench gate type which has a super junction structure.

[0012]The semiconductor device 100 includes a first conductive type semiconductor layer 8, a first region 10, a seventh semiconductor region 12 of a second conductive type, an eighth semiconductor region 14, an empty hole 16, a third semiconductor region 18 of a second conductive type, a second region 20, a fourth semiconductor region 22 of a first conductive type, a first insulator material 24, a third region 30, a second insulator material 32, a fifth semiconductor region 34 of a first conductive type, a first semiconductor region 42 of a first conductive type, a second semiconductor region 44 of a second conductive type, a sixth semiconductor region 46 of a second conductive type, a third insulator material 50, a barrier metal 52, a source electrode 54, and a drain electrode 56.

[0013]Hereinafter, a case in which a first conductive type is an n type, and a second conductive type is a p type will be described as an example. In addition, impurity concentration of a first conductive type is lowered in the sequence of an n+ type, an n type, and an n- type. In the same manner, impurity concentration of a second conductive type is lowered in the sequence of a p+ type, a p type, and a p- type.

[0014]The n type semiconductor layer 8 includes single crystal silicon containing, for example, an n type impurity. The n type semiconductor layer 8 is a drift region of the semiconductor device 100. The n type impurity is, for example, phosphorus (P) or arsenic (As). The n type semiconductor layer 8 is a portion of an n type region of the super junction structure.

[0015]A plurality of first regions 10 are provided so as to alternate with a part of the n type semiconductor layer 8 in a first direction of the semiconductor layer 8. A p type impurity region and a semiconductor material are provided in the plurality of first regions 10. The p type impurity is, for example, boron (B). The semiconductor material is, for example, silicon (Si). The plurality of first regions 10 is a portion of the p type region of the super junction structure.

[0016]The plurality of first regions 10 includes the eighth semiconductor region 14 having the empty hole 16 therein, the seventh semiconductor region 12 of a p type which is provided around the eighth semiconductor region 14, and the third semiconductor region 18 of a p+ type which is provided on the eighth semiconductor region 14 (first region 10). The seventh semiconductor region 12 and the eighth semiconductor region 14 are positioned inside the n type semiconductor layer 8, and the third semiconductor region 18 is positioned on one surface of the n type semiconductor layer 8. The eighth semiconductor region 14 includes Si of an i type (non-doped). A diameter d1 of a lower portion of the empty hole 16 is greater than a diameter d2 of an upper portion of the empty hole 16. That is, the empty hole 16 is formed such that an inner diameter positioned on the third semiconductor region 18 side is smaller than that positioned on the n type semiconductor layer 8 side. The seventh semiconductor region 12 is in contact with, for example, the semiconductor layer 8, the eighth semiconductor region 14, and the sixth semiconductor region 46.

[0017]The second region 20 is provided between the first regions 10 adjacent to each other in the first direction. An n type impurity region, a semiconductor material, and a first insulator material are provided in the second region 20. The first insulator material is, for example, a silicon oxide (SiO2).

[0018]The second region 20 includes the fourth semiconductor region 22 of an n+ type, and the first insulator material 24 provided around the fourth semiconductor region 22. The fourth semiconductor region 22 includes an n type impurity and the semiconductor material. The fourth semiconductor region 22 operates a gate electrode. The first insulator material 24 is in contact with the semiconductor layer 8 and the fourth semiconductor region 22.

[0019]The third region 30 is provided between the first region 10 and the second region 20. For example, the fifth semiconductor region 34 of an n+ type and the second insulator material 32 positioned around the fifth semiconductor region 34 are provided in the third region 30. The second insulator material 32 is positioned in on one surface of the n type semiconductor layer 8, and is in contact with the seventh semiconductor region 12 and the third semiconductor region 18. The second insulator material is, for example, a silicon oxide (SiO2). The second insulator material 32 is in contact with, for example, the fifth semiconductor region 34.

[0020]The first semiconductor region 42 of an n+ type is positioned between the second region 20 and the third region 30, and is provided on one surface of the n type semiconductor layer 8. The first semiconductor region 42 is in contact with the first insulator material 24 and operates as a source region of the semiconductor device 100.

[0021]The second semiconductor region 44 of a p+ type is provided between the third region 30 and the first semiconductor region 42. The second semiconductor region 44 operates as a channel contact region (base contact region) of the semiconductor device 100.

[0022]The sixth semiconductor region 46 of a p type is provided under the first semiconductor region 42 and the second semiconductor region 44 which are positioned between the second region 20 and the third region 30. That is, the sixth semiconductor region 46 is positioned between the n type semiconductor layer 8, and the first semiconductor region 42 and the second semiconductor region 44. The sixth semiconductor region 46 is in contact with the first insulator material 24, and operates as a channel region (base region) of the semiconductor device 100.

[0023]The third insulator material 50 is provided on the n type semiconductor layer 8 in the second region 20. The third insulator material 50 ensures insulation properties between the source electrode 54 and the fourth semiconductor region 22 which will be described below. The third insulator material 50 includes, for example, non-doped silicate glass (NSG) or boro-phospho silicate glass (BPSG).

[0024]The barrier metal 52 is provided on the first region 10, the second region 20, the third region 30, the first semiconductor region 42, the second semiconductor region 44, and the third insulator material 50. The barrier metal 52 prevents aluminum and silicon from diffusing each other due to direct contact between aluminum (Al) for being used for the source electrode 54 which will be described below, and silicon. The barrier metal 52 includes, for example, titanium nitride (TiN), titanium (Ti), or titanium tungsten (TiW).

[0025]The source electrode 54 is provided on the barrier metal 52. The drain electrode 56 is provided under the n type semiconductor layer 8, and is electrically coupled to the n type semiconductor layer 8.

[0026]Next, a fabrication method of the semiconductor device 100 according to the present embodiment will be described. FIG. 2 to FIG. 17 are schematic sectional views of the semiconductor device in the process of the fabrication, based on the fabrication method of the semiconductor device according to the present embodiment.

[0027]In a fabrication method of the semiconductor device 100 according to the present embodiment, a first oxide film is formed on an n type semiconductor layer, a plurality of first regions are formed on the semiconductor layer in a first direction, a p type seventy semiconductor region is formed inside the first region, an eighth semiconductor region is formed inside the first region, an empty hole is formed inside the first region, the surplus eighth semiconductor region formed on the first oxide film is removed, the first oxide film is removed, a second oxide film is formed on the semiconductor layer and the eighth semiconductor region, the second oxide film is removed in a state in which a side wall formed on a side surface of the eighth semiconductor region remains, a ninth semiconductor region of a p type is formed on the semiconductor layer, the eight semiconductor region, and the side wall, the ninth semiconductor region formed on the side wall is removed, a third oxide film is formed on the ninth semiconductor region, a CVD film M is formed on the third oxide film, a first opening having a bottom portion on the ninth semiconductor region and a second opening having a bottom portion inside the semiconductor layer are formed on the semiconductor layer, the second opening is chamfered, a third opening which becomes a third region is formed by removing the CVD film and the third oxide film, a fourth oxide film is formed on the second opening, the third opening, and the ninth semiconductor region, polycrystalline silicon is formed inside the second opening and the third opening, a fourth semiconductor region is formed inside the second region and a fifth semiconductor region of an n type is formed inside the third region by doping an n type impurity in the polycrystalline silicon, a fifth oxide film is formed on the fourth oxide film, the fourth semiconductor region, and the fifth semiconductor region, a third semiconductor region of a p+ type is formed on the eighth semiconductor region, a second semiconductor region of a p+ type is formed between the first region and the second region, a p type impurity is diffused, a first semiconductor region of an n+ type is formed between the first region and the second region, a sixth semiconductor region of a p type is formed under the first semiconductor region and the second semiconductor region, an n type impurity is diffused, a film is formed on the fifth oxide film, thermal processing is performed, a third insulator material is formed on the second region by removing a part of the film, a barrier metal is formed on the first region, the second region, the third region, the first semiconductor region , the second semiconductor region , and the third insulator material, a source electrode is formed on the barrier metal, and a drain electrode is formed under the eighth semiconductor layer 8.

[0028]First, as illustrated in FIG. 2, a first oxide film 60 is formed on the n type semiconductor layer 8 through, for example, a thermal oxide method, the plurality of first regions 10 are formed on the semiconductor layer 8 in the first direction through, for example, reactive ion etching (RIE), and the seventh semiconductor region 8 of a p type is formed inside the first region 10 through, for example, epitaxial growth. Subsequently, the eighth semiconductor region 14 is formed inside the first region 10. At this time, the empty hole 16 having the diameter d1 of a lower portion larger than the diameter d2 of an upper portion is formed inside the first region 10.

[0029]Subsequently, as illustrated in FIG. 3, the surplus eighth semiconductor region 14 formed on the first oxide film 60 is removed by chemical mechanical polishing (CMP) using the first oxide film 60 as a CMP stopper.

[0030]Subsequently, as illustrated in FIG. 4, the first oxide film 60 is removed by using, for example, mixture of hydrofluoric acid and hydrogen peroxide solution.

[0031]Subsequently, as illustrated in FIG. 5, a second oxide film 62 is formed on the semiconductor layer 8 and the eighth semiconductor region 14 through, for example, a thermal oxide method or a chemical vapor deposition (CVD) method.

[0032]Subsequently, as illustrated in FIG. 6, the second oxide film 62 is removed through, for example, RIE, in a state in which the side wall 62 formed on a side surface of the seventh semiconductor region 12 remains.

[0033]Subsequently, as illustrated in FIG. 7, the sixth semiconductor region 46 of a p type is formed on the semiconductor layer 8, the eighth semiconductor region 14, the seventh semiconductor region 12, and the side wall 62 through, for example, epitaxial growth.

[0034]Subsequently, as illustrated in FIG. 8, the sixth semiconductor region 46 of a p type formed on the side wall 62 and the seventh semiconductor region 12 is removed by chemical mechanical polishing (CMP) using the side wall 62 as a CMP stopper.

[0035]Subsequently, as illustrated in FIG. 9, a third oxide film 64 is formed on the sixth semiconductor region 46 of a p type through a thermal oxide method, a CVD film M is formed on the third oxide film 64 through, for example, a CVD method.

[0036]Subsequently, as illustrated in FIG. 10, a first opening 70 having a bottom portion on the sixth semiconductor region 46 is formed on the semiconductor layer 8 by, for example, patterning performed by photolithography and oxide RIE. Subsequently, a second opening 72 having a bottom portion inside the semiconductor layer 8 is formed by silicon RIE. Subsequently, the second opening 72 is chamfered by chemical dry etching (CDE) in order to prevent leakage between a gate electrode and a source electrode. The second opening 72 becomes the second region 20.

[0037]Subsequently, as illustrated in FIG. 11, the CVD film M and the third oxide film 64 are removed. As a result, a third opening 74 is formed. The third opening 74 becomes the third region 30 as will be described below.

[0038]Subsequently, as illustrated in FIG. 12, a fourth oxide film 66 is formed inside the second opening 72 and the third opening 74, and on the sixth semiconductor region 46, through, for example, a thermal oxide method, polycrystalline silicon is formed inside the second opening 72 and the third opening 74 through, for example, a CVD method, and phosphorous (P) which is an n type impurity is doped into the polycrystalline silicon using, for example, phosphoryl chloride POCL3. As a result, the fourth semiconductor region 22 of an n type is formed inside the second region 20, and the fifth semiconductor region 34 of an n type is formed inside the third region 30.

[0039]Subsequently, as illustrated in FIG. 13, a fifth oxide film 68 is formed on the fourth oxide film 66, the fourth semiconductor region 22, and the fifth semiconductor region 34, through, for example, a thermal oxide method.

[0040]Subsequently, as illustrated in FIG. 14, the third semiconductor region 18 of a p+ type is formed on the eighth semiconductor region 14, and the second semiconductor region 44 of a p+ type is also formed between the first region 10 and the second region 20. Thereafter, a p type impurity is diffused by performing first thermal processing, for example, in a temperature higher than or equal to 900°C and lower than or equal to 1100°C. The p type impurity inside the third semiconductor region 18 and a p type impurity inside the seventh semiconductor region are diffused into the eighth semiconductor region 14. In addition, as the p type impurity of the sixth semiconductor region 46 is downwardly diffused, the sixth semiconductor region 46 is downwardly expanded.

[0041]Subsequently, as illustrated in FIG. 15, the first semiconductor region 42 of an n+ type is formed between the first region 10 and the second region 20 by an ion injection method. As a result, the sixth semiconductor region 46 of a p type is formed under the first semiconductor region 42 and the second semiconductor region 44. Thereafter, the n type impurity is diffused by performing second thermal processing, for example, in a temperature higher than or equal to 900°C and lower than or equal to 1100°C. As the p type impurity of the sixth semiconductor region 46 is downwardly diffused, the sixth semiconductor region 46 is downwardly expanded.

[0042]The p type impurity inside the sixth semiconductor region 46 is diffused into the eighth semiconductor region 14 by the first thermal processing or the second thermal processing.

[0043]Subsequently, as illustrated in FIG. 16, a film 50 which includes NSG and BPSG is formed on the fifth oxide film 68, and thermal processing is performed.

[0044]Subsequently, as illustrated in FIG. 17, a part of the film 50 is removed, and thereby the third insulator material 50 is formed on the second region 20.

[0045]Subsequently, the barrier metal 52 is formed on the first region 10, the second region 20, the third region 30, the first semiconductor region 42 of an n type, the second semiconductor region 44 of a p type, and the third insulator material 50, the source electrode 54 is formed on the barrier metal 52, the drain electrode 56 is formed under the semiconductor layer 8, and thereby 100 is obtained.

[0046]Subsequently, actions and effects of the semiconductor device 100 according to the present embodiment will be described.

[0047]As will be described below, in the semiconductor device 100 according to the present embodiment, by using the side wall 62, opening of an upper portion of the empty hole 16 is suppressed, and medical liquid or the like used for a fabrication process does not flow into the empty hole 16. In the fabrication process, a portion in which the side wall 62 is formed is the third region 30 of the semiconductor device 100. That is, the semiconductor device 100 having the third region is fabricated so as to suppress opening of the upper portion of the empty hole 16, and thus it is possible to increase reliability (stability) of the semiconductor device 100. Furthermore, since the third region 30 includes the second insulator material 32, an electric resistance around the third region 30 increases, and it is possible to prevent unintended electrical coupling between the first region 10 and the second region 20.

[0048]In addition, by forming the sixth semiconductor region through epitaxial growth, it is possible to prevent concentration of super junction from being cancelled by heat, compared to formation of a base area performed by ion injection and high temperature diffusion of the related art. Thus, it is possible to fabricate a semiconductor device with a low ON resistance.

[0049]By further including a third semiconductor region including a second conductive type impurity provided on the first region, the second conductive type impurity is also injected from not only the seventh semiconductor region disposed on an upper portion and a side portion of the first region, but also an upper portion of the semiconductor device 100, and thus it is possible to provide the semiconductor device 100 with further stable characteristics.

[0050]By further including the third insulator material 50, insulation properties between the source electrode 54 and the fourth semiconductor region 22 of an n type is ensured.

[0051]Subsequently, actions and effects of the fabrication method of the semiconductor device 100 will be described.

[0052]By allowing formation of the empty hole 16 in the seventh semiconductor region 12 of a p type, it is possible to form more rapidly the eighth semiconductor region 14. However, for example, if the eighth semiconductor region 14 is ground by CMP or the like shortly after the schematic sectional view of the semiconductor device in the process of fabrication illustrated in FIG. 4, the upper portion of the empty hole 16 can be opened. In this case, resist, slurry which is used for CMP, or the like remains inside the empty hole 16, and thus it may be difficult to continue to perform the fabrication process.

[0053]In the fabrication method of the semiconductor device 100 according to the present embodiment the side wall 62 is formed, and thereafter CMP is performed by using the side wall 62 as a CMP stopper. Accordingly, it is possible to prevent the upper portion of the empty hole 16 from being opened. As a result, it is possible to continue to perform the fabrication process.

[0054]Since the d1 is larger than d2, regions in which holes that are generated when the semiconductor device 100 operates moves is widened. Accordingly, the semiconductor device 100 can perform a stable operation.

[0055]As described above, according to the semiconductor device 100 and the fabrication method thereof according to the present embodiment, it is possible to provide a semiconductor device which can stabilize the characteristics of a super junction structure and a fabrication method thereof.

Second Embodiment

[0056]A semiconductor device 200 according to the present embodiment is different from the semiconductor device 100 according to the first embodiment in that the semiconductor device 200 includes a vertical MOSFET of a planar gate type with a super junction structure of. Here, the same portions as in the first embodiment will not be described.

[0057]FIG. 18 is a schematic sectional view of the semiconductor device 200 according to the present embodiment. In the semiconductor device 200 according to the present embodiment and fabrication method thereof, it is also possible to provide a semiconductor device which can stabilize the characteristics of the super junction structure.

[0058]While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first conductive type semiconductor layer;

a plurality of first regions which are positioned to alternate with a portion of the semiconductor layer in a first direction of the semiconductor layer, and includes a second conductive type impurity region;

a second region which is positioned between the first regions in the first direction, and includes a first conductive type impurity region and a first insulator material that is positioned between the first conductive type impurity region and the semiconductor layer; and

a third region which is provided between the first region and the second region, and includes a second insulator material.

2. The device according to Claim 1, further comprising:

a first semiconductor region which includes a first conductive type impurity between the second region and the third region; and

a second semiconductor region which includes a second conductive type impurity between the third region and the first semiconductor region.

3. The device according to Claim 1 or 2, further comprising:

a third semiconductor region which includes a second conductive type impurity that is provided on the first region.

4. The device according to any one of Claims 1 to 3, wherein the first region is provided such that an inner diameter which is positioned on the third semiconductor region side is smaller than an inner diameter which is positioned on the semiconductor layer side.

5. The device according to any one of Claims 1 to 4, further comprising:

a second insulator material which is provided between the second semiconductor region and the third semiconductor region.

6. The device according to any one of Claims 1 to 5, wherein the second region further includes a fourth semiconductor region including a first conductive impurity.

ABSTRACT

According to one embodiment, a semiconductor device includes a first conductive type semiconductor layer; a plurality of first regions which are positioned to alternate with a portion of the semiconductor layer in a first direction of the semiconductor layer, and includes a second conductive type impurity region; a second region which is positioned between the first regions in the first direction, and includes a first conductive type impurity region and a first insulator material that is positioned between the first conductive type impurity region and the semiconductor layer; and a third region which is provided between the first region and the second region, and includes a second insulator material.

Drawings

FIG. 1 to FIG. 18

FIRST DIRECTION